OpenPOWER and Acceleration

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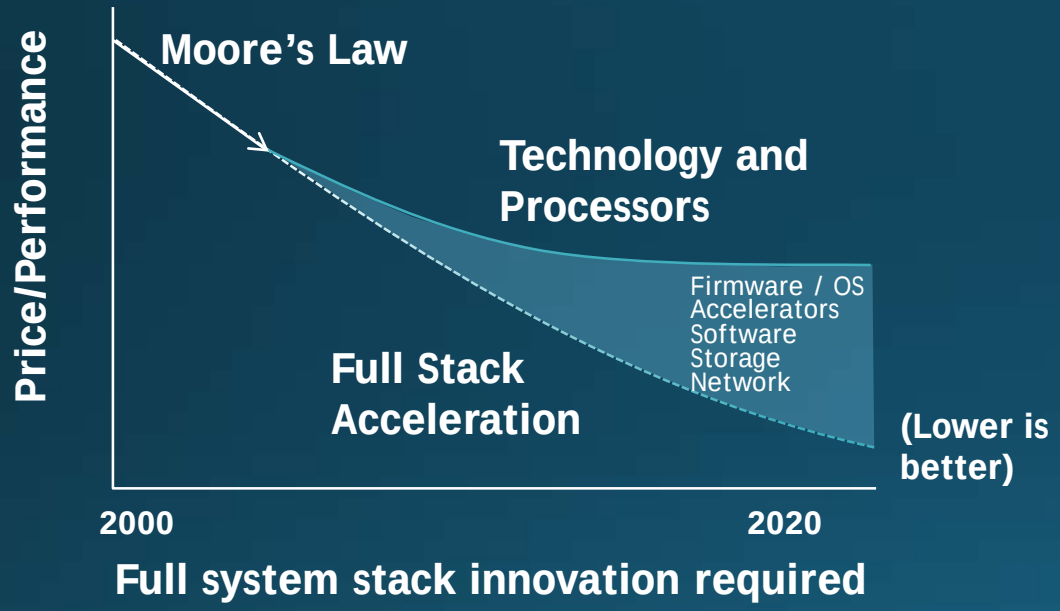
Fundamental forces are accelerating change in our industry

IT innovation can no longer come from just the processor

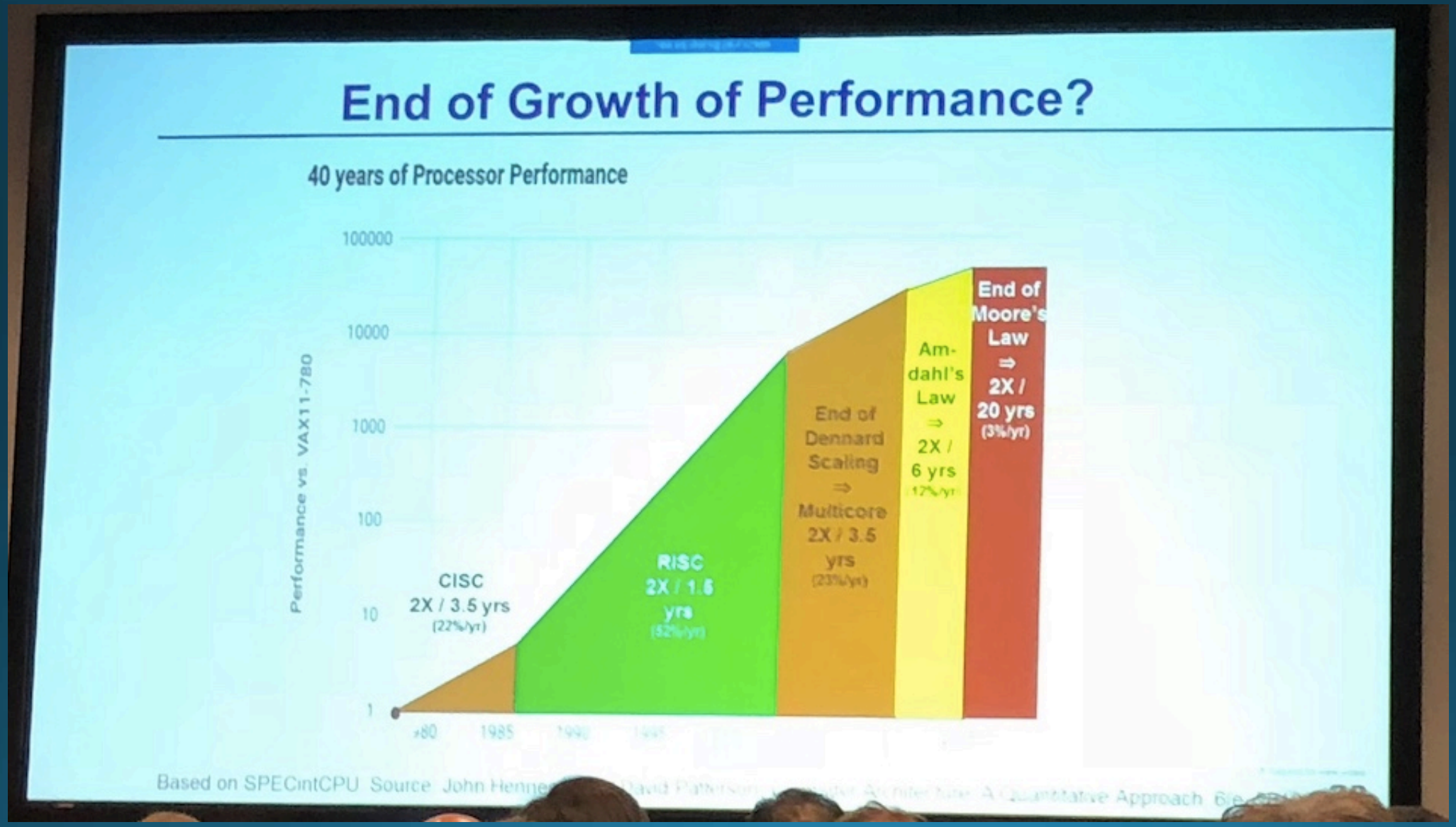


IT consumption models are expanding

- Cognitive
- Custom Hyperscale Data Centers
- Hybrid Cloud
- Open Solutions

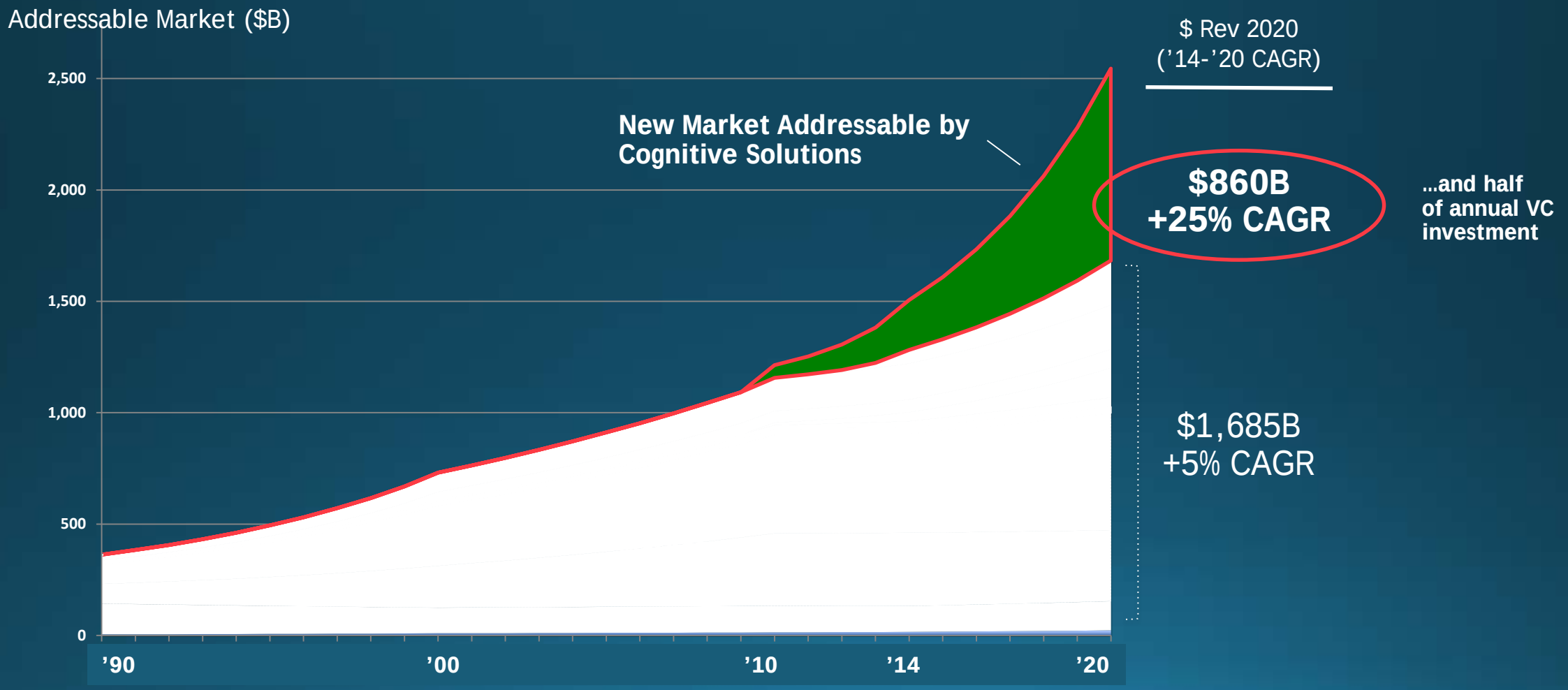
Not only is Moore's Law "coming to an end in practical term, in that chip speeds can be expected to stall, but it is actually likely to roll back in terms of performance …"- William Holt, Intel Executive Vice President and General Manager

Validation from a Legend…



Cognitive Solutions redefine our traditional IT market

Conservatively add 50% to our market by 2020 … likely much more



Creating an Open Processor Ecosystem for POWER (OpenPOWER)

Power Open Source Software Stack Components

Software

Cloud Software

Standard Operating Environment (System Mgmt)

Operating System / KVM

Firmware

Hardware

openstack CLOUD SOFTWARE

Ganglia CAT oVirt

Linux

OpenPOWER Firmware

OpenPOWER Technology

Existing Open Source Software Communities

New OSS Community

System Operating Environment Software Stack

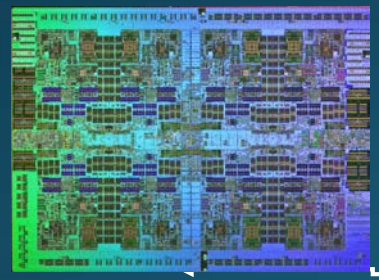
A modern development environment is emerging based on tools and services

40,000 packages now available

Multiple Options to Design with POWER Technology Within OpenPOWER

Hardware

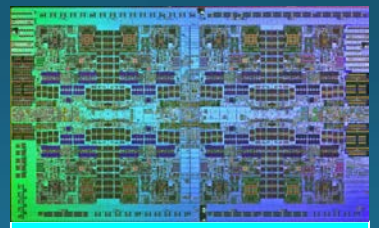
POWER8



CAPI over PCIe

"Standard POWER Products" - 2014

Framework to Integrate System IP on Chip



Customizable

"Custom POWER SoC" - Future

Industry IP License Model

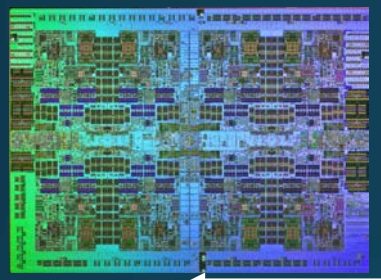
Acceleration Can Have a Bigger Impact on Cost/Performance than Processors

IBM

Multiple Options to Design with POWER Technology Within OpenPOWER

Hardware

POWER8



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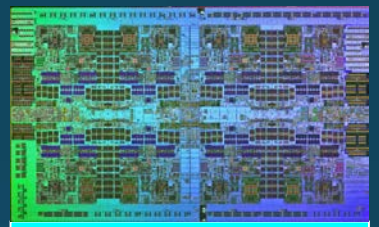

Customizable

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"Standard POWER Products" – 2014

"Custom POWER SoC" – Future

OpenCAPI & NVLink

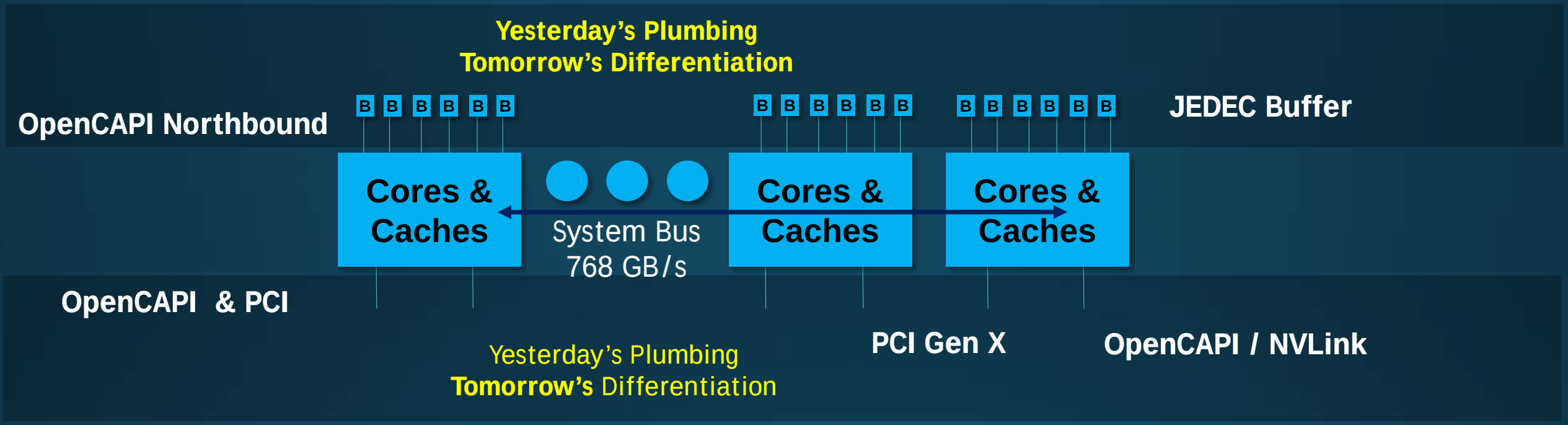
FPGA
GPU
Storage Class Memories
High-performance Networking
Other Stuff…

Proposed POWER Processor Technology and I/O Roadmap

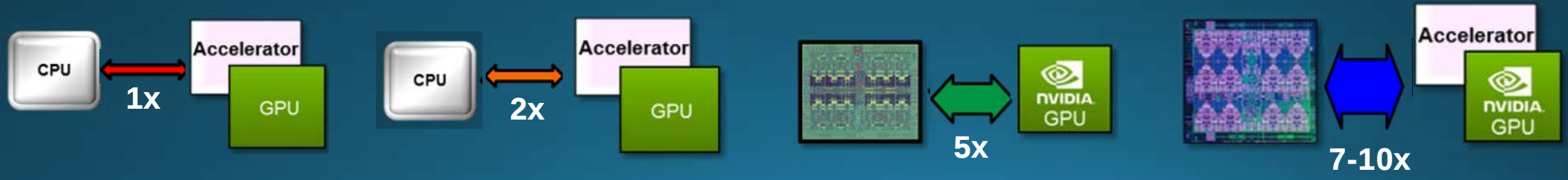
	POWER7 Architecture		POWER8 Architecture		POWER9 Architecture			POWER10
	2010 POWER7 8 cores 45nm New Micro-Architecture New Process Technology	2012 POWER7+ 8 cores 32nm Enhanced Micro-Architecture New Process Technology	2014 POWER8 12 cores 22nm New Micro-Architecture New Process Technology	2016 POWER8 w/ NVLink 12 cores 22nm Enhanced Micro-Architecture With NVLink	2017 P9 SO 24 cores 14nm New Micro-Architecture Direct attach memory New Process Technology	2018 P9 SU 24 cores 14nm Enhanced Micro-Architecture Buffered Memory	2019 P9 w/ Adv. I/O 24 cores 14nm Enhanced Micro-Architecture New Memory Subsystem	2020+ P10 TBD cores New Micro-Architecture New Technology
Sustained Memory Bandwidth	Up To 65 GB/s	Up To 65 GB/s	Up To 210 GB/s	Up To 210 GB/s	Up To 150 GB/s	Up To 210 GB/s	Up To 350 GB/s	Up To 435 GB/s
Standard I/O Interconnect	PCIe Gen2	PCIe Gen2	PCIe Gen3	PCIe Gen3	PCIe Gen4 x48	PCIe Gen4 x48	PCIe Gen4 x48	PCIe Gen5
Advanced I/O Signaling	N/A	N/A	N/A	20 GT/s 160GB/s	25 GT/s 300GB/s	25 GT/s 300GB/s	25 GT/s 300GB/s	32 & 50 GT/s
Advanced I/O Architecture	N/A	N/A	CAPI 1.0	CAPI 1.0 , NVLink 1.0	CAPI 2.0, OpenCAPI3.0, NVLink2.0	CAPI 2.0, OpenCAPI3.0, NVLink2.0	CAPI 2.0, OpenCAPI4.0, NVLink	TBD

Statement of Direction, Subject to Change

Future Evolution of System Architecture



CPU/Accelerator Bandwidth



System bottleneck