An Open Future for Processing Performance – POWER9 & OpenPOWER

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Outline

• Industry Trends
• High Speed Interface Technologies
• POWER Roadmap
• POWER9: Next Generation processor
• Summary
Fundamental forces are accelerating change in our industry

IT innovation can no longer come from just the processor

Full system stack innovation required

IT consumption models are expanding

Cognitive

Custom Hyperscale

Data Centers

Hybrid Cloud

Open Solutions

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OpenPOWER Technology: 2.5x Faster CPU-GPU Connection via NVLink

GPUs Bottlenecked by PCIe Bandwidth From CPU-System Memory

NVLink Enables Fast Unified Memory Access between CPU & GPU Memories
OpenCAPI

• New interface optimized for coherent accelerators and advanced memories
  • 25 Gbit/sec signalling
  • User-level Virtual Addressing & Coherence
  • Range of usage semantics including read/write and atomics

• OpenCAPI Consortium announced October 14
  • Initial members include: AMD, Dell EMC, Google, HPE, IBM, Mellanox, Micron, NVIDIA, Xilinx
  • [www.opencapi.org](http://www.opencapi.org)

• OpenCAPI created as a standalone organization
  • Enable additional CPU architectures to grow coherent acceleration ecosystem
OpenPOWER Technology: Storage Class Memory

Storage Class Memories (SCM)

- First Functioning Demo of SCM in an Enterprise system
- Natively non-volatile ST-MRAM DIMMs (Everspin)
- Avoids NVDIMM complications (DRAM to FLASH and back)
- No Supercaps with umbilicals required
- April 2016 Technology Demo
- October 2016 Application Demo
POWER Processor Roadmap

**POWER6 Architecture**
- 2007 POWER6
  - 2 cores
  - 65nm
  - New Micro-Architecture
  - New Process Technology
- High Frequency
- Enhanced RAS
- Dynamic Energy Management

**POWER7 Architecture**
- 2008 POWER6+
  - 2 cores
  - 65nm+
  - Enhanced Micro-Architecture
  - Enhanced Process Technology
- Large eDRAM L3 Cache
- Optimized VSX
- Enhanced Memory Subsystem

**POWER8 Architecture**
- 2012 POWER7+
  - 8 cores
  - 45nm
  - New Micro-Architecture
  - New Process Technology
- Optimized for Data-Centric Workloads
- Integrated PCIe
- CAPI Acceleration / I/O

**POWER9 Architecture**
- 2014 POWER8
  - 12 cores
  - 22nm
  - New Micro-Architecture
  - New Process Technology
- Scale-Out Datacenter TCO Optimization
- Scale-up performance Optimization
- Acceleration Enhancements to CAPI and NVLINK
- Modularity for OpenPOWER

**Power8+**
- 2016 POWER8 w/ NVLink
  - 12 cores
  - 22nm
  - Enhanced Micro-Architecture With NVLink
  - Direct attach memory
  - New Process Technology

**Future**
- 2017 P9 SO
  - 24 cores
  - 14nm
  - Enhanced Micro-Architecture
  - Buffered Memory
- TBD P9 SU
  - TBD cores
  - 14nm
  - New Micro-Architecture
  - Foundry Technology

**POWER10**
- 2018 - 20 P8/9 SO
  - 10nm - 7nm
  - Existing Micro-Architecture
  - OpenPOWER Ecosystem Design
  - Targeting Partner Markets & Systems
  - Leveraging Modularity

**OpenPOWER Ecosystem Design**
- New Features and Functions

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Price, performance, feature and ecosystem innovation

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POWER9 SO with Advanced Accelerator Attach

- 24 newly designed POWER9 cores
  - Leveraging execution slices for improved performance on cognitive, analytic, and big-data applications
- Large, low-latency, eDRAM cache for big datasets
- Global Foundries 14HP finFET technology with eDRAM
- Cloud-focused innovation in Energy Efficiency, Security, and Quality of Service
- State-of-the-art IO subsystem using PCIe Gen4

- Leadership platforms for hardware acceleration
  - High bandwidth, GPU interconnect (NV link2.0)
  - Next-generation CAPI2.0 interface for coherent accelerator and storage attach
  - On-chip compression & cryptography accelerators
  - New 25Gb/s advanced accelerator attach bus
- 1st chip in POWER9 family
  - Optimized for 2 socket scale out servers & hyperscale datacenters
  - DDR4 direct attach memory channels
- Full POWER9 family will address a broad range of scale out & enterprise servers
POWER9 Processor Family

Four targeted implementations

**SMP scalability / Memory subsystem**

**Scale-Out – 2 Socket Optimized**

Robust 2 socket SMP system

Direct Memory Attach

- Up to 8 DDR4 ports
- Commodity packaging form factor

**Scale-Up – Multi-Socket Optimized**

Scalable System Topology / Capacity

- Large multi-socket
- Additional lanes of 25G Link (96 total)

Buffered Memory Attach

- 8 Buffered channels

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**Core Count / Size**

**SMT4 Core**

- 24 SMT4 Cores / Chip
- Linux Ecosystem Optimized

**SMT8 Core**

- 12 SMT8 Cores / Chip
- PowerVM Ecosystem Continuity

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Advancements in POWER9 SO

• Significant performance increase compared to POWER8

• Direct-attach DDR4 Memory Subsystem
  - Reduce cost and energy consumption by removing memory buffers
  - Enable increased server density

• Better accelerator attach
  - NVLink 2.0: More bandwidth and capability
  - CAPI 2.0: Extend POWER8 CAPI ecosystem to PCIe 4.0 Speed with enhanced capability
  - OpenCAPI: New interface for higher performing accelerators and advanced memories
Summary

• Fundamental forces are accelerating change in our industry
• IT consumption models are expanding and innovation can no longer come from just the processor
• Workloads have unique acceleration needs
• OpenCAPI provides new interface optimized for coherent accelerators and advanced memories
• OpenPOWER + OpenCAPI – Open standards providing platform for innovation and collaboration
• POWER9
  • Leadership platform for hardware acceleration
  • POWER9 family will address broad range of scale out and enterprise servers