OpenPOWER and the Roadmap Ahead

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Revolutionizing the Datacenter
Quarter Century of POWER
Legacy of Leadership Innovation
Driving Client Value


Modern UNIX Era

POWER8
POWER7/7+
POWER6
POWER5/5+
POWER4/4+
POWER3-630
POWER2 P2SC
POWER1
RSC
RS64IV Sstar
RS64III Pulsar
RS64II North Star
RS64I Apache
Cobra A10
Muskie A35
Power Systems
# POWER Processor Roadmap

## Focus on Enterprise Technology and Performance Driven

<table>
<thead>
<tr>
<th>POWER6 Architecture</th>
<th>POWER7 Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>2007 POWER6</td>
<td>2008 POWER6+</td>
</tr>
<tr>
<td>2 cores 65nm</td>
<td>2 cores 65nm+</td>
</tr>
<tr>
<td>New Micro-Architecture</td>
<td>Enhanced Micro-Architecture</td>
</tr>
<tr>
<td>New Process Technology</td>
<td>New Process Technology</td>
</tr>
</tbody>
</table>

- **High Frequency**
- **Enhanced RAS**
- **Dynamic Energy Management**

| 2010 POWER7          | 2012 POWER7+        |
| 8 cores 45nm         | 8 cores 32nm        |
| New Micro-Architecture | Enhanced Micro-Architecture |
| New Process Technology | New Process Technology |

- **Large eDRAM L3 Cache**
- **Optimized for Data-Centric Workloads**
- **Optimized VSX**
- **Enhanced Memory Subsystem**

## Focus on Scale-Out and Enterprise Cost and Acceleration Driven

<table>
<thead>
<tr>
<th>POWER8 Architecture</th>
<th>POWER9 Architecture</th>
</tr>
</thead>
<tbody>
<tr>
<td>2014 POWER8</td>
<td>2017 P9 SO</td>
</tr>
<tr>
<td>12 cores 22nm</td>
<td>24 cores 14nm</td>
</tr>
<tr>
<td>New Micro-Architecture</td>
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</table>

- **Optimized for Data-Centric Workloads**
- **Integrated PCIe**
- **CAPI Acceleration / I/O**

<table>
<thead>
<tr>
<th>2016 POWER8 w/ NVLink</th>
<th>2017 P9SO w/ NVLink</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 cores 22nm</td>
<td>14nm</td>
</tr>
<tr>
<td>New Micro-Architecture With NVLink</td>
<td>Direct attach memory</td>
</tr>
<tr>
<td>New Process Technology</td>
<td>New Process Technology</td>
</tr>
</tbody>
</table>

- **Scale-Out Datacenter TCO Optimization**
- **Scale-up performance Optimization**
- **Acceleration Enhancements to CAPI and NVLINK**
- **Modularity for OpenPOWER**

## Future

<table>
<thead>
<tr>
<th>POWER10</th>
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<tr>
<td>2020+</td>
</tr>
<tr>
<td>New Micro-Architecture</td>
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<td>New Technology</td>
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</tbody>
</table>

## Partner Chip POWER8/9

- **2018 - 20 P8/9 SO**
- **10nm - 7nm**

- **Existing Micro-Architecture**
- **Foundry Technology**
- **OpenPOWER Ecosystem Design**
- **Targeting Partner Markets & Systems**
- **Leveraging Modularity**

## TBD

- **Existing Micro-Architecture**
- **Foundry Technology**
- **New Features and Functions**

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**Price, performance, feature and ecosystem innovation**
Cores
- 12 cores / 8 threads per core
- TDP: 130W and 190W
- 64K data cache, 32K instruction cache

Accelerators
- Crypto & memory expansion
- Transactional Memory

Caches
- 512 KB SRAM L2 / core
- 96 MB eDRAM shared L3

Memory Subsystem
- Memory buffers with 128MB Cache
- ~70ns latency to memory

Bus Interfaces
- Durable Memory attach Interface (DMI)
- Integrated PCIe Gen3
- SMP Interconnect for up to 4 sockets

Virtual Addressing
- Accelerator can work with same memory addresses that the processors use
- Pointers de-referenced same as the host application
- Removes OS & device driver overhead

Hardware Managed Cache Coherence
- Enables the accelerator to participate in “Locks” as a normal thread
- Lowers Latency over IO communication model

Server Class Memories (SCM)
- First Functioning Demo of SCM in an Enterprise system
- 15x better than SSD
- Natively non-volatile ST-MRAM DIMMs (Everspin)
- Avoids NVDIMM complications (DRAM to FLASH and back)
- No Supercaps with umbilicals required

Coherent Accelerator Processor Interface (CAPI)
- 6 Hardware Partners developing with CAPI

Over 20 CAPI Solutions
- All listed here http://ibm.biz/powercap

Examples of Available CAPI Solutions
- IBM Data Engine for NoSQL
- DRC Graphfind analytics
- Erasure Code Acceleration for Hadoop
Two tracks to challenge and win:

1. The Open Road Test
   - Port and optimize for OpenPOWER
   - Go faster with accelerators (optional)

2. The Spark Rally
   - Train an accelerated DNN and recognize objects with greater accuracy
   - Show you can scale with Spark

Key Dates

Register today
openpower.devpost.com

Sun May 1st:
Submission periods opens

Tue Aug 2nd:
Submission period closes

Grand prizes include a trip to Supercomputing 2016
Other prizes include iPads, Apple Watches

Join the conversation at #OpenPOWERSummit

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POWER8 with NVLink

- NVLink High Speed CPU <-> GPU Interconnect
- 160+ GigaBytes per second bi-directional
- 5-12x faster than PCIe Gen3 x16

- Nvlink Accelerator Lab
  accellab@us.ibm.com

Nvidia GPU

NVLINK

Memory Interface Control

Memory

DMI

CAPI/PCI

IBM & Partner Devices

SMP

22nm SOI, eDRAM, 15 ML 650mm2

Nvlink Accelerator Lab

accellab@us.ibm.com

Minsky

NVLink POWER Systems

Zoom
24 newly designed POWER9 cores
  • Leveraging execution slices for improved performance on cognitive, analytic, and big-data applications

Large, low-latency, eDRAM cache for big datasets

Global Foundries 14HP finFET technology with eDRAM

Cloud-focused innovation in Energy Efficiency, Security, and Quality of Service

State-of-the-art IO subsystem using PCIe Gen4

Leadership platforms for hardware acceleration
  • High bandwidth, GPU interconnect (NV link2.0)
  • Next-generation CAPI2.0 interface for coherent accelerator and storage attach
  • On-chip compression & cryptography accelerators
  • New 25Gb/s advanced accelerator attach bus

1st chip in POWER9 family
  • Optimized for 2 socket scale out servers & hyperscale datacenters
  • DDR4 direct attach memory channels

Full POWER9 family will address a broad range of scale out & enterprise servers
POWER Processor Roadmap

Denser Roadmap
  Not tied to technology
  More teams developing

Performance and cost/performance leadership

Leadership accelerator attach technologies including
  GPUs
  Advanced Storage
  Advanced Networking
  FPGAs

Expanded focus includes Enterprise and Hyperscale datacenters

All of these technologies will be made available to our partners