POWER8:
The first OpenPOWER processor

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OpenPOWER is about choice in large-scale data centers

- The choice to differentiate
  - build workload optimized solutions
  - use best-of-breed components from an open ecosystem

- The choice to innovate
  - collaborative innovation in open ecosystem
  - with open interfaces

- The choice to grow
  - delivered system performance
  - new capabilities instead of technology scaling

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Why Power and Why Now?

- Power is optimized for server workloads
- Power8 was optimized to simplify application porting
- Power8 includes CAPI, the Coherent Accelerator Processor Interconnect
  - Building on a long history of IBM workload acceleration
POWER8 Processor

Cores
• 12 cores (SMT8) ➔ 96 threads per chip
• 2X internal data flows/queues
• 64K data cache, 32K instruction cache

Caches
• 512 KB SRAM L2 / core
• 96 MB eDRAM shared L3
• Up to 128 MB eDRAM L4 (off-chip)

Accelerators
• Crypto & memory expansion
• Transactional Memory
• VMM assist
• Data Move / VM Mobility
• Coherent Accelerator Processor Interface (CAPI)
POWER8 Core

• Up to eight hardware threads per core (SMT8)
• 8 dispatch
• 10 issue
• 16 execution pipes:
  • 2 FXU, 2 LSU, 2 LU, 4 FPU, 2 VMX, 1 Crypto, 1 DFU, 1 CR, 1 BR
• Larger Issue queues (4 x 16-entry)
• Larger global completion, Load/Store reorder queue
• Improved branch prediction
• Improved unaligned storage access
• Improved data prefetch
POWER8 Architecture

- High-performance LE support
  - Foundation for a new ecosystem
- Organic application growth
  - Instruction Fusion
- Workload optimized
  - Power SIMD Extensions
  - Coherent Accelerator Processor Interface
- Parallel programming productivity
  - Transactional Memory
- Cloud ready
  - Cloud Mode
  - Reduced context switch overhead
  - Improved Interrupt performance
- Dynamic System Optimization
  - Performance Monitoring
  - Dynamic Code Optimization

Power evolution

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Up to 2.7x performance across key workloads vs. other 24-core Scale-Out Systems

Java – SPECjbb2013 (Max-jOPS)
- 2.7x Performance

SPECint_rate2006
- 1.8x Performance

SPECfp_rate2006
- 2x Performance

Source: Hot Chips 26
Workload-optimized acceleration with coherent accelerators

- Attached accelerators
  - Accelerate workloads with functions that are not a good fit for traditional general purpose CPU

- Coherent integration in system architecture
  - Data sharing
  - Programming
  - Performance

**Typical I/O Model Flow**

**Flow with a Coherent Model**

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Workload-optimized acceleration

- On-chip integrated accelerators (SoC design)
  - Compute accelerator (Cell BE)
  - Compression (P7+)
  - Encryption (P7+)
  - Random number generation (P7+)
  - ...

- SoC design offers highest integration, but...
  - New chip design to introduce new accelerator
  - Long time to market
  - Requires very high volumes
Integrate accelerators into system architecture with standardized, coherent protocol
- CAPI functional protocol
- PCIe signaling protocol

Modular interface enables third parties to provide high value-add components

Create workload-optimized innovative solutions
- Faster time to market
- Lower bar to entry
- Variety of implementation options
  - FPGAs, ASICs

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CAPI accelerator programming

Virtual Addressing
- Accelerator can work with the same virtual memory addresses that the processors use.
- CAPI shares page tables and provides address translation.
- Pointers de-referenced same as the host application.
- Peer-to-peer programming between CPU and accelerator with in-memory data sharing.

Hardware Managed Coherence
- No need for memory pinning.
- Data fetched by accelerator based on accelerator application flow.
- Accelerator participates in locks.
- Low latency communication.

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POWER8: expanding choice for data formats

- **Big-Endian**: Most Significant Byte First
  - Traditional enterprise server data format
  - The standard internet data format ("network byte order")
  - Process five decades of database content
  - Protect investment into data storage and curation

- **Little-Endian**: Least Significant Byte First
  - Traditional small system format (PC, mobile)
  - High-volume hardware components often little-endian
  - Participate in rich standard ecosystem
  - Simplify application portability for those seeking to upgrade to Power
Summary

- POWER8 introduce traditional microarchitecture improvements
  - More Instruction level parallelism
  - More Data level parallelism
  - Larger caches and queues
  - Best-in-class systems performance for scale-out and scale-up

- New foundational capabilities for OpenPOWER
  - High-performance little- and big-endian
    - Improved integration of industry standard ecosystem hardware
    - Improved application portability to OpenPOWER
  - CAPI enables system architects to extend processor capabilities
    - Create a broad range of workload optimized offerings

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