Enabling Coherent FPGA Acceleration

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Nallatech
Overview

- Nallatech at a Glance
- Coherent Attached Accelerators...So what’s new?
- How CAPI Works compared to PCIe Accelerators
- IBM/Nallatech’s CAPI Developer Kit Overview
- CAPI to PMC NVMe Demo
Nallatech at a glance

Server qualified accelerator cards featuring FPGAs, network I/O and an open architecture software/firmware framework

Design Services/Application Optimization

- Leading supplier of FPGA solutions
- Energy-efficient High Performance Heterogeneous Computing
- Real-time, low latency network and I/O processing
- Altera OpenCL partner
- OpenPower Foundation Member

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Coherent Accelerators...So what’s new?

- Decade of Coherent “In Socket” Accelerators
  - Hyper-Transport, FSB & QPI
- Not commercially successful, Why?
  - Proprietary “In Socket” attached
  - Server mechanical fit challenges
  - Need to give up processor socket
  - Proprietary Specification
  - Licensing Issues
  - Always lagging 6-12 Month cadence
Coherent Accelerators...So what’s new?

- **IBM’s Coherent Accelerator**
  - Processor Interface, CAPI, Resolves ALL these Issues
  - Already Commercialized
  - Industry Standard PCIe Attached
  - PCIe – No Mechanical Challenges
  - Processors use all available sockets
  - OpenPower & well documented
  - Free & simple OpenPower Licensing
  - In sync with POWER & PCIe Cadence

“In Socket” Coherent Accelerators

CAPI PCIe Cards

POWER8 Modules

Industry Standard Server Configuration
How CAPI Works

CAPI FPGA Accelerator – (NOTE: Based on a Standard PCIe Accelerator)

- Acceleration Portion: Data or Compute Intensive, Storage or External I/O
- Sharing the same memory space
  Accelerator is a peer to POWER8 Core
- Application Portion: Data Set-up, Control
CAPI technology connections

- Proprietary hardware to enable coherent acceleration
- Operating system enablement
  - Ubuntu LE
  - Libcxl function calls
- Customer application and accelerator

- Application sets up data and calls the accelerator functional unit (AFU)
- AFU reads and writes coherent data across the PCIe and communicates with the application
  - PSL cache holds coherent data for quick AFU access

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Issues with PCIe Accelerators

- Prior to CAPI, an application called a device driver to utilize an FPGA Accelerator.
- The device driver performed a memory mapping operation.

3 versions of the data (not coherent).
1000s of instructions in the device driver.
Benefit of Coherent accelerators

- With CAPI, the FPGA shares memory with the cores
- Greatly simplifies programming model

1 coherent version of the data. No device driver call/instructions.
CAPI vs. PCIe Device Driver: Data Prep

Typical PCIe Model Flow: Total ~13µs for data prep

```
DD Call → Copy or Pin Source Data → MMIO Notify Accelerator → Acceleration → Poll / Interrupt Completion → Copy or Unpin Result Data → Ret. From DD Completion
```

- DD Call: 300 Instructions, 7.9µs
- Copy or Pin Source Data: 10,000 Instructions
- MMIO Notify Accelerator: Application Dependent, but Equal to below
- Acceleration: 3,000 Instructions
- Poll / Interrupt Completion: 4.9µs, 1,000 Instructions
- Copy or Unpin Result Data: 1,000 Instructions
- Ret. From DD Completion: Total 0.36µs

Flow with a Coherent Model: Total 0.36µs

```
Shared Mem. Notify Accelerator → Acceleration → Shared Memory Completion
```

- Shared Mem. Notify Accelerator: 400 Instructions, 0.3µs
- Acceleration: Application Dependent, but Equal to above
- Shared Memory Completion: 100 Instructions, 0.06µs

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Nallatech CAPI Attached FPGA Accelerator

- Nallatech’s 385 Card is the CAPI FPGA accelerator card
- Collaborated with IBM & Altera through OpenPower
- Offering CAPI Developer Kit for Power8

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<td>IBM CAPI Power Service Layer (PSL) (Encrypted FPGA IP)</td>
<td>Altera Quartus FPGA Tools</td>
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<td>'Memcopy' Example</td>
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<td>Also Required</td>
<td>Power 8 System (IBM Model 8247-21L or 8247-22L)</td>
<td>CAPI Enabled O/S (initially Ubuntu 14.10 LE from Canonical)</td>
<td>HDL Simulator (i.e. Cadence, Mentor, Synopsis)</td>
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Nallatech 385 FPGA Accelerator

Low cost, low power, high performance

- Half height, half length PCIe form factor (NIC-size)
- Altera Stratix V FPGA: A7
- PCIe Gen3x8 or CAPI host interface
- 2 SFP+ network IO ports
- 2 banks of DDR3 SDRAM: up to 32GB total

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CAPI Developer Kit, Power8 Server Options

- **IBM Power8 System S812L/(S822L)**
  - 2U server with 1/(2) 10 or 12 Core 3.42 or 3.02GHz Processor(s)
  - 80/96 MB L3 Cache per socket + 512KB L2 Cache/Core
  - Up to 512GB/(1TB) Memory @ 192/(384) GBytes/s Memory Bandwidth
  - Up to 12/(14) Disk/SSD Drives – RAID optional
  - 2/(4) PClex16 + 4/(5) PClex8 Low Profile Slots – 2/(4) CAPI Enabled
CAPI - Getting Started Resources

- More details at nallatech.com/capi
- Discuss your application at nallatech.com/support

Learn More About CAPI

Take a Deeper Technical Dive

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CAPI to PMC NVMe Demo

- NVMe SSD to 385 CAPI FPGA Accelerator
- Accelerating Data Analytic operations
- Minimal CPU Core Loading
- See Demo at Booth 1010